Page 21, last paragraph, line 3, change "region" to --body 11--; and

Page 21, last paragraph, line 4, change "region" (last occurrence) to --first drift region 217--.

IN THE CLAIMS:

Claim 1, delete without prejudice, and substitute therefor the following new claims.

--31. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;

a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;

a fourth semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said third semiconductor region;

a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said third semiconductor region;

A3 cont

an insulator layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body and material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein

when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor region and said fourth semiconductor region;

said semiconductor body having a first ON resistance in a first current flow path therethrough between said second and third semiconductor regions, and said fifth semiconductor region providing a second ON resistance in a second current flow path along the surface of said semiconductor body from said second semiconductor region through said channel and said fourth and fifth semiconductor regions to said third semiconductor region, so that said fifth semiconductor region serves to provide a current flow path in parallel with said first current flow path, thereby effectively reducing the total ON resistance of the overall current flow path between said second and third semiconductor regions.

A3 cont

~~32.~~ 2 A semiconductor device according to claim ~~31~~ 1, wherein a peripheral edge of said gate electrode is aligned with a peripheral edge of said fifth semiconductor region.

~~33.~~ 3 A semiconductor device according to claim ~~31~~ 1, wherein said fourth semiconductor region overlaps said first semiconductor region.

4 1
~~34.~~ A semiconductor device according to claim ~~31~~, wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

5
~~35.~~ A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

A3 cont

a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;

a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;

a fourth semiconductor region of said second conductivity type formed in said third surface portion of said semiconductor body and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said first and third semiconductor regions;

a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said first and third semiconductor regions;

an insulator layer formed on said first surface of said semiconductor body; and

A3 Cont

a gate electrode formed on said insulator layer so as to overlie material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein

when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor region and said fourth semiconductor region.

36. A semiconductor device according to claim 34 wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

37. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said second conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof and defining a second PN junction with said semiconductor body;

a third semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said third semiconductor region being contiguous with said second semiconductor region;

a fourth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said third semiconductor region and defining therewith a fourth PN junction;

an insulator layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body, that portion of said semiconductor body lying beneath said gate electrode serving as a channel region of said device, said gate electrode being applied with a gate voltage for inducing a conductive channel through said channel region;

A3 cont

said device being reverse-biased, so that a first depletion region extends from said third PN junction into said third semiconductor region and said semiconductor body and a second depletion region extends from said fourth PN junction into said third semiconductor region and said fourth semiconductor region;

said semiconductor body having a first ON resistance in a first current flow path therethrough between said first and second semiconductor regions, and said fourth semiconductor region providing a second ON resistance, less than said first ON resistance, in a second current flow path along the surface of said semiconductor body from said first semiconductor region through said channel and said third and fourth semiconductor regions to said second semiconductor region, so that said fourth semiconductor region serves to provide a reduced resistance current flow path in parallel with said first current flow path,

thereby effectively reducing the total ON resistance of the overall current flow path between said first and second semiconductor regions; and

wherein the impurity concentration said fourth semiconductor region is such that said fourth semiconductor is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said third semiconductor region.

8

38. A high voltage MOS transistor comprising:

A3 cont

a semiconductor substrate of a first conductivity type having a surface,

a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,

an extended drain region of the second conductivity type extending laterally each way from said drain pocket to surface-adjoining positions,

a surface adjoining top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and the surface-adjoining positions,

said top layer of material and said substrate being subject to application of a reverse-bias voltage,

an insulating layer on the surface of the substrate and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

9

39. A high voltage MOS transistor according to claim 8, wherein said extended drain region has an impurity concentration greater than $1x10^{12}$ cm^{-2}.

A3 cont

10

40. A high voltage MOS transistor according to claim 8, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor substrate, said ohmic contact region overlapping said top layer of material.

11

41. A high voltage MOS transistor comprising:

semiconductor material of a first conductivity type having a surface,

a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the surface of said semiconductor material,

an extended drain region of the second conductivity type extending laterally from said drain pocket to a surface-adjoining position,

a surface adjoining top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and said surface-adjoining position,

said top layer of material and said semiconductor material being subject to application of a reverse-bias voltage,

an insulating layer on the surface of said semiconductor material and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from a semiconductor material region thereunder containing a channel that extends laterally between the source pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

A3 cont

12
~~42.~~ A high voltage MOS transistor according to claim ~~41,~~ 11 wherein said extended drain region extends in a plurality of different directions from said drain pocket to respective plural surface adjoining positions.

13
~~43.~~ A high voltage MOS transistor according to claim ~~41,~~ 11 wherein said extended drain region surrounds said drain pocket and extends to a surrounding surface adjoining position.

19 ~~44.~~ A high voltage MOS transistor according to claim 11 ~~41~~, wherein said drain pocket comprises a first relatively deep pocket of a first impurity concentration and a second relatively shallow pocket formed in a surface portion of said first relatively deep pocket and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

15 ~~45.~~ A high voltage MOS transistor according to claim 11 ~~41~~, wherein said extended drain region has an impurity concentration greater than $1x10^{12}$ cm^{-2}.

16 ~~46.~~ A high voltage MOS transistor according to claim 11 ~~41~~, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top layer of material.

A3 Cont

17 ~~47.~~ A high voltage field effect transistor device comprising:

semiconductor material of a first conductivity type having a surface;

a source region of a second conductivity type formed in a first surface portion of said semiconductor material;

a drain region of said second conductivity type formed in a second surface portion of said semiconductor material spaced apart from said first surface portion by a third surface portion therebetween;

an extended drain region of said second conductivity type extending from said drain region beneath a first portion of said third surface portion of said semiconductor material, to adjoin a second portion of said third surface portion of said semiconductor material, spaced apart from said second surface portion of said semiconductor material, by said first portion of said third surface portion of said semiconductor material;

a surface region of said first conductivity type formed in said first portion of said third surface portion of said semiconductor material;

an insulating layer disposed on said surface of said semiconductor material, so as to overlie a third portion of said third surface portion of said semiconductor material between the second portion of said third surface portion of said semiconductor material and said first surface portion of said semiconductor material; and

A3 Cont

a gate electrode disposed on that portion of said insulating layer overlying said third portion of said third surface portion of said semiconductor material, and wherein said surface region and said semiconductor material are subject to the application of a reverse bias voltage.

18

48. A high voltage field effect transistor device according to claim 47, wherein said extended drain region extends laterally in a plurality of different directions from said drain region to adjoin said second portion of said third surface portion of said semiconductor material and to adjoin a fifth surface portion of said semiconductor material.

17

19
~~49.~~ A high voltage field effect transistor device according to claim 17, wherein said extended drain region surrounds said drain region and extends to a surrounding surface-adjoining portion of said semiconductor material.

20
~~50.~~ A high voltage field effect transistor device according to claim 17, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

A3 cont

21
~~51.~~ A high voltage field effect transistor device according to claim 17, wherein said extended drain region has an impurity concentration greater than $1x10^{12}$ cm^{-2}.

22
~~52.~~ A high voltage field effect transistor device according to claim 17, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said surface region.

~~53~~ 83. An integrated MOS/JFET transistor device comprising an insulated gate field effect transistor and a double-sided junction field effect transistor integrated together in semiconductor substrate which contains a source region and a drain region ~~formed therein~~, and a dual channel path formed in said semiconductor material between said source and drain regions, said dual channel path comprising an insulated gate-controlled channel region having a first conductivity type in the presence of a channel-inducing gate voltage, said insulated gate controlled channel region being contiguous with a double-sided junction channel region of said first conductivity type, and wherein said source region adjoins said insulated gate-controlled channel region and said drain region adjoins said double-sided channel region.

~~54~~ 84. An integrated MOS/JFET transistor device according to claim ~~53~~ 83, wherein said insulated gate-controlled channel region comprises a surface portion of said semiconductor material adjoining said source region, and wherein said double-sided junction channel region comprises an extended drain region extending laterally from said drain region beneath a top gate region to said surface portion of said semiconductor material, an underlying portion of said semiconductor material extending beneath and adjoining said extended drain region and forming a bottom gate, said top gate region and said bottom gate forming respective PN junctions with said double-sided junction channel region.

25 ~~85~~. An integrated MOS/JFET transistor device according to claim ~~53~~ 23, wherein said extended drain region and said double-sided junction channel region surround said drain region and extend to a surrounding surface-adjoining position.

26 ~~56~~. An integrated MOS/JFET transistor device according to claim ~~53~~ 23, wherein said extended drain region and said double, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

A3 cont

27 ~~57~~. An integrated MOS/JFET transistor device according to claim ~~53~~ 23, wherein said extended drain region and said double, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate.

28 ~~58~~. An integrated MOS/JFET transistor device according to claim ~~53~~ 23, wherein said extended drain region has an impurity concentration greater than $1x10^{12}$ cm^{-2}.

29. A high voltage MOS transistor comprising:

semiconductor material of a first conductivity type having a surface;

source and drain regions of a second conductivity type adjoining spaced apart portions of the surface of said semiconductor material;

an extended drain region of said second conductivity type extending laterally from said drain region through said semiconductor material to a surface-adjoining portion of the surface of said semiconductor material;

a top gate semiconductor layer of said first conductivity type adjoining said drain region and adjoining said extended drain region along the surface of said semiconductor material to said surface-adjoining portion of the surface of said semiconductor material, said top gate semiconductor layer and said semiconductor material being subject to the application of a reverse-bias voltage;

A3 cont'd

an insulating layer on the surface of the semiconductor material and covering at least that portion of the surface of said semiconductor material between said source region and said surface-adjoining portion of said extended drain region; and

a gate electrode disposed on said insulating layer and being electrically isolated from that portion of the surface of said semiconductor material thereunder which forms a channel laterally between said source region and said surface-adjoining portion of said extended drain region, said gate electrode controlling, by field-effect, the flow of current thereunder through said channel.

60. A high voltage MOS transistor according to claim 59, wherein said extended drain region extends laterally each way from said drain region to surface-adjoining portions of the surface of said semiconductor material, and wherein said top gate semiconductor layer extends laterally in a plurality of different directions from said drain region and adjoins said extended drain region along the surface of said semiconductor material to said surface-adjoining portions of the surface of said semiconductor material.

61. A high voltage MOS transistor according to claim 59, wherein said extended drain region surrounds said drain region and extends to a surrounding surface adjoining position.

62. A high voltage MOS transistor according to claim 59, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

63. A high voltage MOS transistor according to claim 59, wherein said extended drain region has an impurity concentration greater than $1x10^{12}$ cm^{-2}.

34 29
64. A high voltage MOS transistor according to claim 59, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate layer.

35
65. A high voltage diode comprising:

a semiconductor material of a first conductivity type having a surface,

a first, surface-adjoining region of a second conductivity type;

a second surface-adjoining region of said first conductivity type spaced apart from said first, surface-adjoining region;

A3 Cont a third region of said second conductivity type extending laterally from said first, surface-adjoining region; and

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining region.

36 35
66. A high voltage diode according to claim 65, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

37 67. A high voltage diode according to claim 35 65, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

38 68. A high voltage diode according to claim 35 65, wherein said third region has an impurity concentration greater than $1x10^{12}$ cm^{-2}.

A3 Cont 39 69. A lateral bipolar transistor having a high voltage base-collector diode comprising:

semiconductor material of a first conductivity type having a surface and forming a base of said bipolar transistor,

a first, surface-adjoining collector region of a second conductivity type forming a base-collector junction with said semiconductor material;

a second surface-adjoining base region of said first conductivity type spaced apart from said first, surface-adjoining collector region;

a third, extended collector region of said second conductivity type extending laterally from said first, surface-adjoining collector region, so that said base-collector junction extends laterally from said first, surface adjoining collector region;

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining extended collector region; and

a fifth, surface-adjoining emitter region of said second conductivity type formed in said second surface-adjoining base region and defining therewith an emitter-base junction.

40 ~~70.~~ A lateral bipolar transistor according to claim 39 ~~69,~~ wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

A3 Cont

41 ~~71.~~ A lateral bipolar transistor according to claim 39 ~~69,~~ wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

42 ~~72.~~ A lateral bipolar transistor according to claim 39 ~~69,~~ wherein said third, extended collector region has an impurity concentration greater than $1x10^{12}$ cm^{-2}.

REMARKS

The specification has been amended to conform with the Amendment filed July 13, 1990 in parert application Serial No. 242,405.

Original claims 1-30 have been replaced by new claims 31-72. Of these newly presented claims, claims 31-37 correspond to those claims filed in the Amendments of July 13, 1990 and January 25, 1991, in parent application Serial No. 242,405, and incorporating the Amendments of the Examiner's Amendment dated February 22, 1991. New claims 38-72 embody further definitions of subject matter for which patent protection is sought.

With respect to newly added claims 38-72, to the extent that 37 C.F.R. 1.607(c) is applicable, please be advised that claim 38, although not identically copied, is considered to be generic to the invention defined in claim 1 of U.S. Patent No. 4,811,075 to Eklund. Claims 41, 47 and 59 are also considered to be generic to the invention defined in claim 1 of the patent to Eklund, 4,811,075.

U.S. Patent No. 4,823,173, of which application Serial No. 242,405, filed September 8, 1988 is a continuation-in-part, has a filing date of January 7, 1986, the present application being a continuation of application Serial No. 242,405, it is respectfully submitted that the effective filing date of the above-identified claims is the filing date of parent Patent 4,823,173, or January 7, 1986. This filing date antedates the filing date of April 24, 1987 of the above-identified Eklund patent, 4,811,075.

Early examination of the present application is earnestly solicited.

To the extent necessary, Applicants petition for an Extension of Time under 37 C.F.R. 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 05-1323 (118/28508CO) and please credit any excess fees to such deposit account.

Respectfully submitted,

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SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
07/705,509	05/24/91	BEASOM J	118/28508C0

EXAMINER
POTTER, R

ART UNIT: 2508
PAPER NUMBER: 7

DATE MAILED: 03/26/92

EVENSON, MANN, EDWARDS, LENAHAN & MC KEOWN
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PALM BAY, FL 32905

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), — days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☒ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, Form PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 2-72 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☒ Claims 1 have been cancelled.
3. ☒ Claims 31-36, 41-52 and 54-72 are allowed.
4. ☒ Claims 2-30, 37-38, 40, and 53 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable. ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed on _____, has been ☐ approved. ☐ disapproved (see explanation).
12. ☐ Acknowledgment is made of the claim for priority under U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

SN: 07/705509
PTOL-326 (Rev. 9-89)

EXAMINER'S ACTION

FCS1688988

The disclosure is objected to because of the following informalities: Figures 1 and 3, which are described in the specification as representing known devices should be labeled "PRIOR ART". Appropriate correction is required.

Claims 2 - 30 are rejected under 35 U.S.C. § 112, fourth paragraph, as being of improper dependent form for failing to further limit the subject matter of a previous claim. Claim 1 has been canceled by preliminary amendment, however claims 2 - 30 which are dependent on claim 1 have not been canceled. These claims cannot remain in the application dependent upon a canceled claim.

Claims 37, 38, 40, and 53 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Line 2 of claim 37 recites "a semiconductor body of the first conductivity type". Line 8 - 9 recite "a second semiconductor region of said first conductivity type". Lines 11 - 12 describe the second semiconductor region as "defining a second PN junction with said semiconductor body". This is unclear as the second semiconductor region and the semiconductor

body are both of the first conductivity type.

Line 14 of claim 38 and line 5 of claim 40 refer to "said top layer of material". There is no antecedent basis for this layer.

Lines 4 - 5 of claim 53 recite "a source region, and a drain region formed therein." It is unclear how the drain region is formed in the source region,

Claim 36 does not further limit the claims. Claim 36 is dependent on claim 34 which recites the identical limitations. The examiner believes that the applicant intended for claim 36 to be dependent on claim 35. If this is the case, claim 36 should be amended to make this clear.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 38 - 46 are rejected under 35 U.S.C. § 102(b) as being anticipated by Eklund.

Eklund reveals a high voltage MOS transistor. In his

device, an insulated gate, field effect transistor and a double sided, junction-gate field effect transistor are connected in series on the same chip to form a high voltage MOS transistor. An extended drain region is formed on top of a substrate of opposite conductivity type material. A top layer of material having a conductivity type opposite that of the extended drain and similar to that of the substrate covers only an intermediate portion of the extended drain which has ends contacting a silicon dioxide layer thereabove. The top layer can either be connected to the substrate or left floating. Figure 1 shows drain contact 16 contacting region 24 of n+ conductivity type. Contiguous to region 24 is region 26 of N- conductivity type which extends under gate 17 toward source 21 also of n+ conductivity type.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Colak reveals a lateral double diffused MOS transistor which includes an intermediate semiconductor layer of the same conductivity type as the channel region which extends laterally from the channel region to beneath the drain contact region of the device. This intermediate semiconductor layer substantially improves the punchthrough and avalanche breakdown characteristics of the device.

Nakagawa et al. reveal a MOSFET having a drain voltage deflection function. The MOSFET includes a base layer of a first conductivity type selectively formed in the surface layer of a high resistance semiconductor layer, and a source layer of a second conductivity type formed in the surface of the base layer. A drain layer of the second conductivity type is formed on the front or rear surface layer of the high resistance semiconductor layer so as to be separated from the base layer of by a predetermined distance. A gate insulating film is formed on the base layer, and a gate electrode is formed on the gate insulating film. A voltage detection terminal layer of the second conductivity type independent from the source layer is formed in the base layer. A voltage detection electrode is in contact with the voltage detection terminal layer.

Claim 53 would be allowable if rewritten or amended to overcome the rejection under 35 U.S.C. § 112.

Claims 39 and 54 - 58 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 31 - 36, 47 - 52 and 59 - 72 are allowable over the prior art of record. Claims 31 - 35 correspond to claims 31 - 34 and 36 of application serial number 07/242,405, which is now abandoned.

Any inquiry concerning this communication should be directed to Roy Potter at telephone number (703) 308 - 4864.

RP Roy Potter
March 22, 1992

Rolf Hille
ROLF HILLE
SUPERVISORY PATENT EXAMINER
ART UNIT 253

PTO FORM 948
(REV. 5-90)

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

ATTACHMENT TO PAPER NUMBER 2.

APPLICATION NUMBER 705509

NOTICE OF DRAFTSMAN'S PATENT DRAWING REVIEW

THE PTO DRAFTSMEN REVIEW ALL ORIGINALLY FILED DRAWINGS REGARDLESS OF WHETHER THEY WERE DESIGNATED AS INFORMAL OR FORMAL.

The drawings filed 5/24/91

A. ☐ are approved.

B. ☒ are objected to under 37 CFR 1.84 for the reason(s) checked below. The examiner will require submission of new, corrected drawings at the appropriate time. Corrected drawings must be submitted according to the instructions listed on the back of this Notice.

1. Paper and ink. 37 CFR 1.84(a)

☒ Sheet(s) 1-14 Poor. copy machine marks on paper cb.

2. Size of Sheet and Margins. 37 CFR 1.84(b)

Acceptable Paper Sizes and Margins

Margin	Paper Size: 8 1/2 by 14 inches	8 1/2 by 13 inches	DIN size A4 21 by 29.7 cm.
Top	2 inches	1 inch	2.5 cm.
Left	1/4 inch	1/4 inch	2.5 cm.
Right	1/4 inch	1/4 inch	1.5 cm.
Bottom	1/4 inch	1/4 inch	1.0 cm.

☒ Proper Size Paper Required. paper undersized
All Sheets Must be Same Size.
Sheet(s) 1-14

☐ Proper Margins Required.
Sheet(s) _____
☐ TOP ☐ RIGHT
☐ LEFT ☐ BOTTOM

3. Character of Lines. 37 CFR 1.84(c)

☒ Lines Pale or Rough and Blurred; must be dark & sharp
Fig(s) 1-14

☐ Solid Black Shading Not Allowed.
Fig(s) _____

4. Hatching and Shading. 37 CFR 1.84(d)

☐ Shade Lines are Required.
Fig(s) _____

☐ Criss-Cross Hatching Not Allowed.
Fig(s) _____

☐ Double Line Hatching Not Allowed.
Fig(s) _____

☐ Parts in Section Must be Hatched.
Fig(s) _____

5. Reference Characters. 37 CFR 1.84(f)

☒ Numerals & letters must be uniform & sharp & well defined. Reference Characters Poor or Incorrectly Sized.
Fig(s) 1-14

☐ Reference Characters Placed Incorrectly.
Fig(s) _____

6. Views. 37 CFR 1.84(i) & (j)

☐ Figures Must be Numbered Properly.
_____

☐ Figures Must Not be Connected.
Fig(s) _____

7. ☐ Photographs Not Approved.

8. ☒ Other. -fig. legends must be uniform (fig 1-14)
-descriptive matter (fig. 7, 11-14)

Telephone inquiries concerning this review should be directed to the Chief Draftsman at telephone number (703) 557-6404.

TC
Reviewing Draftsman

6/12/91
Date

TO SEPARATE, HOLD TOP AND BOTTOM EDGES, SNAP–APART AND DISCARD CARBON

FORM PTO-892 (REV. 3-78) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

NOTICE OF REFERENCES CITED

SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
07/705509	2508	2

APPLICANT(S): Beasom

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A	4,994,904	2/19/91	Nakagawa et al.	357	38	5/24/89
	B	4,994,889	2/19/91	Takeuchi et al.	357	55	12/2/87
	C	4,811,075	3/7/89	Eklund et al	357	46	4/24/87
	D	4,626,879	12/2/86	Colak	357	23.8	8/15/85
	E	4,628,341	12/9/86	Thomas	357	23.8	9/27/85
	F						
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG	PERTINENT PP. SPEC.
	L								
	M								
	N								
	O								
	P								
	Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	
S	
T	
U	

EXAMINER: [signature] DATE: 3/21/92

* A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05 (a).)

FCS1688995

118/28508C0

#3/B

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: JAMES D. BEASOM

SERIAL NO.: 07/705,509 ART UNIT: 2508

FILED: May 24, 1992 EXAMINER: R. Potter

FOR: HIGH VOLUME LATERAL SEMICONDUCTOR DEVICE

BQ. 7/7/92 8/13/92

RESPONSE

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

June 26, 1992

Sir:

In reply to the Office Action dated March 26, 1992, the following Amendments and Remarks are respectfully submitted in connection with the above-identified application.

AMENDMENTS

In the Specification:

Before the first line, delete the Amendment of May 24, 1991 and substitute the following: --This a continuation of application, Serial No. 242,405, filed September 8, 1988, now abandoned which, in turn, is a continuation-in-part of application, Serial No. 831,384, filed January 7, 1986, now U.S. Patent No. 4823173, issued April 18, 1989.--

In the Claims:

Please amend the Claims as follows:

Claim 36, Line 1, change "34" to --35,--.

Claim 37, Line 8, change "first" to --second--.

Claim 38, Line 10, between "adjoining" and "layer" insert --,top--.

Claim 53, Line 4, Delete ","; Line 5, delete "formed therein".

REMARKS

The Specification and Claims have been amended, and a proposed correction to the drawings has been submitted. Reconsideration of this application, in light of the foregoing amendments and following remarks is respectfully requested.

On a separate red-lined sheet, the addition of "prior art" labels to Figures 1 and 3 is proposed. Approval of these corrections is earnestly solicited. Upon completion of the prosecution of the present application, and an indication that the application is otherwise in condition for allowance, Applicant will file formal drawings which include the proposed corrections to Figures 1 and 3.

The rejection of Claims 2-30, under the provisions of 35 U.S.C. 112, for the reasons set forth in the second paragraph on Page 2 of the outstanding Office Action, is respectfully traversed.

The present application was filed pursuant to the provisions of 37 C.F.R. 1.60, on May 24, 1991. The filing included an Item 4 in which original Claims 2-30 were canceled before calculating the filing fee. A review of the application papers filed May 24, 1991 is respectfully requested.

The rejection of Claims 37, 38, 40, and 53, under the provisions of 35 U.S.C. 112, for the reasons set forth in the paragraphs on Pages 2 and 3 of the outstanding Office Action, is respectfully traversed.

Claim 37 has been amended to delineate the fact that the second semiconductor region is of the second conductivity type. Withdrawal of the rejection of Claim 37 is respectfully requested.

Claim 38 has been amended to recite that the surface adjoining layer is a surface adjoining, top layer. Withdrawal of the rejection of Claim 38 is respectfully requested.

Claim 53 has been amended to recite the fact that the semiconductor substrate contains a source region and a drain region. The objected-to phraseology has been deleted from the Claim. Withdrawal of the rejection of Claim 53 is respectfully requested.

The objection to Claim 36 is well taken. Claim 36 has been amended to depend upon Claim 35, as proposed in the outstanding Office Action.

The rejection of Claims 38-46, under the provisions of 35 U.S.C. 102 (b) as being anticipated by the patent to Eklund, is respectfully traversed.

On Page 26 of remarks of Applicant's Preliminary Amendment, filed May 24, 1991, reference was made to the fact that the present application has an effective filing date of January 7, 1986, which antedates the filing date of the patent to Eklund 4,811,075. The insertion before the first line of the Specification has been amended to specify this fact. Since the present application has an effective filing date which antedates the filing date of the patent to Eklund, the patent is not available as a reference under 35 U.S.C. (b). Withdrawal of the rejection under 35 U.S.C. 102, is, accordingly, respectfully requested.

In the event that the remarks accompanying Applicant's Preliminary Amendment of May 24, 1991 were overlooked, they are restated below. Please note that Applicant considers Claims 38-72, to the extent that 37 C.F.R. 1.607 is applicable, to be generic to the invention defined in Claim 1 of U.S. Patent No. 4,811,075 to Eklund.

> "The Specification has been amended to conform with the Amendment filed July 13, 1990 in parent application Serial No. 242,405.
>
> Original Claims 1-30 have been replaced by new Claims 31-72. Of these newly presented Claims, Claims 31-37 correspond to those Claims filed in the Amendments of July 13, 1990 and January 25, 1991, in parent application Serial No. 242,405, and incorporating the Amendments of the Examiner's Amendment dated February 22, 1991. New Claims 38-72 embody further definitions of subject matter for which patent protection is sought.
>
> With respect to newly added Claims 38-72, to the extent that 37 C.F.R. 1.607 (c) is applicable, please be advised that Claim 38, although not identically copied, is considered to be generic to the invention defined in Claim 1 of U.S. Patent No. 4,811,075 to Eklund. Claims 41, 47, and 59 are also considered to be generic to the invention defined in Claim 1 of the

patent to Eklund, 4,811,075.

U.S. Patent No. 4,823,173, of which application Serial No. 242,405, filed September 8, 1988 is a continuation-in-part, has a filing date of January 7, 1986, the present application being a continuation of application Serial No. 242,405, it is respectfully submitted that the effective filing date of the above-identified Claims is the filing date of parent Patent 4,823,173, or January 7, 1986. This filing date antedates the filing date of April 24, 1987, of the above-identified Eklund patent, 4,811,075."

Favorable reconsideration of this Application and appropriate action, in accordance with current patent practices with respect to the Claims remaining in the Application, are respectfully requested.

To the extent necessary, Applicant petitions for an Extension of Time under 37 C.F.R. 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 05-1323 118/28508 and please credit any excess fees to such deposit account.

Respectfully submitted,

CEW:tw
(407) 725-4760
(202) 457-9090
pat*28508.rsp

Charles E. Wands
Registration No. 25,649
EVENSON, WANDS, EDWARDS, LENAHAN & MCKEOWN

118/28508C0

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: JAMES D. BEASOM

SERIAL NO.: 07/705,509 ART UNIT: 2508

FILED: May 24, 1992 EXAMINER: R. Potter

FOR: HIGH VOLUME LATERAL SEMICONDUCTOR DEVICE

CERTIFICATE OF MAILING

Honorable Commissioner of
Patents and Trademarks

Sir:

I hereby certify that a Response in reply to the Office Action dated March 26, 1992, to which a reply is currently due on or before June 26, 1992, in connection with the above-identified application is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Honorable Commissioner of Patents and Trademarks, Washington, D.C. 20231 on June 26, 1992.

Charles E. Wands
Reg. No. 25,649
EVENSON, WANDS, EDWARDS,
LENAHAN & MCKEOWN

FIGURE 1

(PRIOR ART)

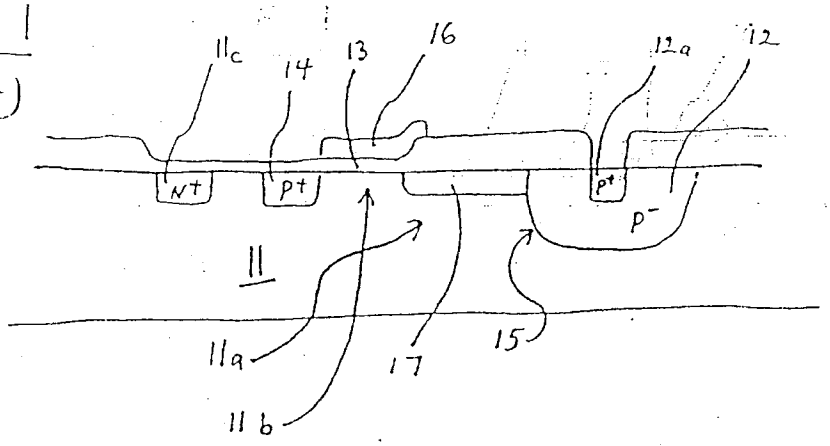
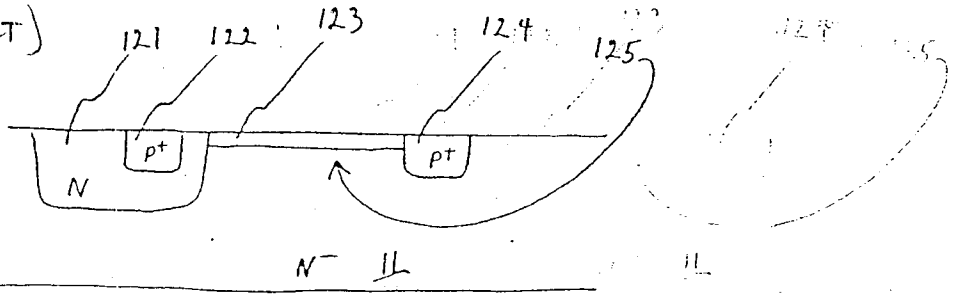


FIGURE 3

(PRIOR ART)



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/705,509	05/24/91	BEASOM	J 119/28508C0

EXAMINER: POTTER, R

ART UNIT: 2508 | PAPER NUMBER: 4

DATE MAILED: 10/20/92

EVENSON, WANDS, EDWARDS, LENAHAN & MC KEOWN
5240 BABCOCK STREET, NE, STE. 206
PALM BAY, FL 32905

NOTICE OF ALLOWABILITY

PART I.

1. ☒ This communication is responsive to Amendment filed 6/29/92
2. ☒ All the claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice Of Allowance And Issue Fee Due or other appropriate communication will be sent in due course.
3. ☒ The allowed claims are 31-72
4. ☐ The drawings filed on _____ are acceptable.
5. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has [_] been received. [_] not been received. [_] been filed in parent application Serial No. _____, filed on _____.
6. ☐ Note the attached Examiner's Amendment.
7. ☐ Note the attached Examiner Interview Summary Record, PTOL-413.
8. ☐ Note the attached Examiner's Statement of Reasons for Allowance.
9. ☐ Note the attached NOTICE OF REFERENCES CITED, PTO-892.
10. ☐ Note the attached INFORMATION DISCLOSURE CITATION, PTO-1449.

PART II.

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" indicated on this form. Failure to timely comply will result in the ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

1. ☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.
2. ☒ APPLICANT MUST MAKE THE DRAWING CHANGES INDICATED BELOW IN THE MANNER SET FORTH ON THE REVERSE SIDE OF THIS PAPER.
   a. ☒ Drawing informalities are indicated on the NOTICE RE PATENT DRAWINGS, PTO-948, attached hereto or to Paper No. 2 CORRECTION IS REQUIRED.
   b. ☐ The proposed drawing correction filed on _____ has been approved by the examiner. CORRECTION IS REQUIRED.
   c. ☐ Approved drawing corrections are described by the examiner in the attached EXAMINER'S AMENDMENT. CORRECTION IS REQUIRED.
   d. ☒ Formal drawings are now REQUIRED.

Any response to this letter should include in the upper right hand corner, the following information from the NOTICE OF ALLOWANCE AND ISSUE FEE DUE: ISSUE BATCH NUMBER, DATE OF THE NOTICE OF ALLOWANCE, AND SERIAL NUMBER.

Attachments:
- _ Examiner's Amendment
- _ Examiner Interview Summary Record, PTOL-413
- _ Reasons for Allowance
- _ Notice of References Cited, PTO-892
- _ Information Disclosure Citation, PTO-1449
- _ Notice of Informal Application, PTO-152
- _ Notice re Patent Drawings, PTO-948
- _ Listing of Bonded Draftsmen
- _ Other

ROLF HILLE
SUPERVISORY PATENT EXAMINER
ART UNIT 250

SN: 07/705509

PTOL-37 (REV. 4-89) *

USCOMM-DC 89-3789

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: Box ISSUE FEE
COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

EVENSON, WANDS, EDWARDS, LENAHAN &
MC KEOWN
5240 BABCOCK STREET, NE, STE. 206
PALM BAY, FL 32905

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

☒ Note attached communication from the Examiner
☐ This notice is issued in view of applicant's communication filed _____

SERIES CODE/SERIAL NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
07/705,509	05/24/91	042	POTTER, R	2508	10/20/92

First Named Applicant: BEASOM, JAMES D.

TITLE OF INVENTION: HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

	ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2	118/28508C0	257-335.000	H31	UTILITY	NO	$1170.00	01/21/93

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY Status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:
A. If the Status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
B. If the Status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:
A. Pay FEE DUE shown above, or
B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B of this notice should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by a charge to deposit account, Part B should be completed and returned. If you are charging the ISSUE FEE to your deposit account, Part C of this notice should also be completed and returned.

III. All communications regarding this application must give series code (or filing date), serial number and batch number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees.

PTOL-85 (REV 12-88)(OMB Clearance is pending)

PATENT AND TRADEMARK OFFICE COPY

#5

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: James D. Beason

Serial No.: 07/705,~~035~~ 504 Group: 2508

Filed: 05/24/91 Examiner: R. Potter

For: HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

Batch No.: H31

4190
10-22-92
Stout
Potter
2508

NOTICE RE:
CHANGE OF FIRM NAME

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

March 12, 1993

Sir:

Please be advised of the following change of firm name of the undersigned attorney. All future communications in connection with the above-identified application are to be directed to the following firm address:

LAW OFFICES OF CHARLES E. WANDS
5240 Babcock Street, N.E.
Suite 306
Palm Bay, Florida 32905

TELEPHONE: (407) 725-4760

Respectfully submitted

Charles E. Wands
Registration No. 25,649
Attorney of Record

PART B - ISSUE FEE TRANSMITTAL

MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 2 through 6 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advanced orders and notification of maintenance fees will be mailed to addressee entered in Block 1 unless you direct otherwise, by: (a) specifying a new correspondence address in Block 3 below; or (b) providing the PTO with a separate "FEE ADDRESS" for maintenance fee notifications with the payment of Issue Fee or thereafter. **See reverse for Certificate of Mailing.**

MAIL ROOM JAN 25 1993 PAT. & TRADEMARK OFF.

1. CORRESPONDENCE ADDRESS

EVENSON, WANDS, EDWARDS, LENAHAN & MC KEOWN
5240 BABCOCK STREET, NE, STE. 206
PALM BAY, FL 32905

2. INVENTOR(S) ADDRESS CHANGE (Complete only if there is a change)

INVENTOR'S NAME
Street Address
City, State and ZIP Code
CO-INVENTOR'S NAME
Street Address
City, State and ZIP Code

☐ Check if additional changes are on reverse side

SERIES CODE/SERIAL NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
07/705,509	05/24/91	042	POTTER, R 2508	10/20/92

First Named Applicant: BEASOM, JAMES D.

TITLE OF INVENTION: HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

	ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2	110/28508C0	257-335.000	H31	UTILITY	NO	$1170.00	01/21/93

3. Further correspondence to be mailed to the following:

Law Offices of
Charles E. Wands
5240 Babcock Street, N.E., Ste. 306
Palm Bay, Florida 32905

4. For printing on the patent front page, list the names of not more than 3 registered patent attorneys or agents OR alternatively, the name of a firm having as a member a registered attorney or agent. If no name is listed, no name will be printed.

Evenson, Wands, Edwards Lenahan & McKeown
2
3

DO NOT USE THIS SPACE

07/705,509 08-0870 110 142 1,170.00CH
07/705,509 08-0870 110 551 40.00CH

5. ASSIGNMENT DATA TO BE PRINTED ON THE PATENT (print or type)

(1) NAME OF ASSIGNEE:
Harris Corporation

(2) ADDRESS: (City & State or Country)
Melbourne, Florida

(3) STATE OF INCORPORATION, IF ASSIGNEE IS A CORPORATION
Florida

A. ☐ This application is NOT assigned.

☒ Assignment previously submitted to the Patent and Trademark Office.

☐ Assignment is being submitted under separate cover. Assignments should be directed to Box ASSIGNMENTS.

PLEASE NOTE: Unless an assignee is identified in Block 5, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

6a. The following fees are enclosed:

☐ Issue Fee ☐ Advanced Order - # of Copies ____ (Minimum of 10)

6b. The following fees should be charged to:

DEPOSIT ACCOUNT NUMBER 08-0870
(Enclose Part C)

☒ Issue Fee ☒ Advanced Order - # of Copies 16 (Minimum of 10)

☒ Any Deficiencies in Enclosed Fees

The COMMISSIONER OF PATENTS AND TRADEMARKS is requested to apply the Issue Fee to the application identified above.

(Signature of party in interest of record)	(Date)
Charles Wands, 25,649	1/21/93

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

TRANSMIT THIS FORM WITH FEE-CERTIFICATE OF MAILING ON REVERSE

PTOL-85B (REV 12-88)(OMB Clearance is pending)

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:

Box ISSUE FEE
Commissioner of Patents and Trademarks
Washington, D.C. 20231

on January 21, 1993
(Date)

Cathy Nicholson
(Name of person making deposit)

(Signature)

1/21/93
(Date)

Note: If this certificate of mailing is used, it can only be used to transmit the Issue Fee. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawings, must have its own certificate of mailing.

This form is estimated to take 20 minutes to complete. Time will vary depending upon the needs of the individual applicant. Any comments on the amount of time you require to complete this form should be sent to the Office of Management and Organization, Patent and Trademark Office, Washington, D.C. 20231 and to the Office of Information and Regulatory Affairs, Office of Management and Budget, Washington, D.C. 20503.

VERSE PTOL-85B (REV 12-88)(OMB Clearance is pending)

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address : COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/705,509	05/24/91	BEASOM J	118/2850810

4102/0811

LAW OFFICES OF CHARLES E. WANDS
5240 BABCOCK STREET, NE, STE. 206
SUITE 306
PALM BAY, FL 32905

EXAMINER	
POTTER,R	
ART UNIT	PAPER NUMBER
2508	7

DATE MAILED: 08/11/93

NOTICE OF ABANDONMENT

This application is abandoned in view of:

1. ☐ Applicant's failure to respond to the Office letter, mailed _____ .
2. ☐ Applicant's letter of express abandonment which is in compliance with 37 C.F.R. 1.138.
3. ☐ Applicant's failure to timely file the response received _____ within the period set in the Office letter.
4. ☐ Applicant's failure to pay the required issue fee within the statutory period of 3 months from the mailing date of _____ of the Notice of Allowance.
   - ☐ The issue fee was received on _____ .
   - ☐ The issue fee has not been received in Allowed Files Branch as of _____ .

   In accordance with 35 U.S.C. 151, and under the provisions of 37 C.F.R. 1.316(b), applicant(s) may petition the Commissioner to accept the delayed payment of the issue fee if the delay in payment was unavoidable. The petition must be accompanied by the issue fee, unless it has been previously submitted, in the amount specified by 37 C.F.R. 1.17 (l), and a verified showing as to the causes of the delay.

   If applicant(s) never received the Notice of Allowance, a petition for a new Notice of Allowance and withdrawal of the holding of abandonment may be appropriate in view of Delgar Inc. v. Schuyler, 172 U.S.P.Q. 513.
5. ■ Applicant's failure to timely correct the drawings and/or submit new or substitute formal drawings by 11/21/93 as required in the last Office action.
   - ☐ The corrected and/or substitute drawings were received on _____ .
6. ☐ The reason(s) below.

Drawing Processing Branch
Roderick Jones
703-305-8067

PTO-1432 (REV. 5-83)

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address : COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/705,509	05/24/91	REASOM J	118/2850800

4102/0902
LAW OFFICES OF CHARLES E. WANDS
5240 BABCOCK STREET, NE, STE. 206
SUITE 306
PALM BAY, FL 32905

POTTER, REXAMINER	
ART UNIT	PAPER NUMBER
2508	8

DATE MAILED: 09/02/93

NOTICE OF RESCINDED ABANDONMENT

☐ In response to your communication filed _____

■ Through inadvertence, a Notice of Abandonment was mailed in the above identified application. The Notice of Abandonment is hereby rescinded. The issue fee receipt will be mailed within six weeks.

Manager, Publishing Division
Office of Publications

Issuing Processing Branch
Roderick Jones
703-305-8067

FORM PTOL-393 (Rev. 4-83)

9200 B #9

118/28508CO

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: James D. Beasom

Serial No.: 07/705,509 Group: 2508

Filed: 05/24/91 Examiner: R. Potter

For: HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

Batch No.: H31

REQUEST FOR WITHDRAWAL OF ABANDONMENT

Honorable Commissioner of
Patents and Trademarks

August 20, 1993

Sir:

Further to receipt of a NOTICE OF ABANDONMENT dated August 11, 1993, in connection with the above-identified application, Applicant respectfully requests that the Notice of Abandonment be withdrawn based on the following comments and attachments.

The above-identified application is deemed to be abandoned by the U.S. Patent and Trademark Office, by failure to submit formal drawings in reply to the Notice of Allowability dated October 20, 1993.

Applicant submitted seven (7) sheets of formal drawings on March 12, 1993, including a LETTER TO DRAFTSMAN and a PETITION FOR EXTENSION OF TIME, also dated March 12, 1993. Copies of these papers as submitted to the U.S. Patent and Trademark Office are attached.

As well, a "return-receipt" postcard was submitted, which postcard has been received back by Applicant. The "return-receipt" postcard indicates receipt by the MAIL ROOM of the U.S. Patent and Trademark Office on March 19, 1993, copy attached.

In reviewing our files, it was discovered that the U.S. Serial Number on the paper work dated March 12, 1993, i.e., LETTER TO DRAFTSMAN, and "PETITION FOR EXTENSION OF TIME, was incorrectly typed. The incorrect Serial Number on the paper work submitted March 12, 1993 reads 07/705,059, when in fact the correct U.S. Serial Number is 07/705,509. The "509" was incorrectly typed as "059".

Therefore, Applicant respectfully submits a copy of the paper work as submitted on March 12, 1993, indicating the incorrect Serial Number, 07/705,059, as typed. We have marked in pencil through the "059" portion of the Serial Number, correcting it with the prefix "509".

Copies of the formal drawings as submitted are attached as well for incorporation into the file.

Thus, it is respectfully requested that the ABANDONMENT of this application be withdrawn, and that the application be allowed to issue.

To the extent necessary, Applicant(s) petition for an Extension of Time under 37 C.F.R. 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 23-0385 (118/28508CO) and please credit any excess fees to such deposit account.

Respectfully submitted,

LAW OFFICES OF CHARLES E. WANDS

CEW:cn
(407) 725-4760

Charles E. Wands
Reg. No. 25,649

118/28508CO

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: James D. Beasom

Serial No.: 07/705,509 Group: 2508

Filed: 05/24/91 Examiner: R. Potter

For: HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

Batch No.: H31

CERTIFICATE OF MAILING

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

August 20, 1993

Sir:

I hereby certify that copies: LETTER TO DRAFTSMAN, PETITION FOR EXTENSION OF TIME, and seven (7) sheets of formal drawings as submitted on March 12, 1993, in connection with the above-identified application is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Honorable Commissioner of Patents and Trademarks, Washington, D.C. 20231 on August 20, 1993.

Charles E. Wands
Reg. No. 25,649

118/28508CO

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: James D. Beasom

Serial No.: 07/705,059 509 Group: 2508

Filed: 05/24/91 Examiner: R. Potter

For: HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

Batch No.: H31

LETTER TO DRAFTSMAN

Honorable Commissioner of
Patents and Trademarks

March 12, 1993

Sir:

In reply to the outstanding NOTICE OF ALLOWABILITY dated October 20, 1992, requesting the submission of new formal drawings, enclosed please find seven (7) sheet(s) of formal drawings to correct the objections raised in the NOTICE OF DRAFTSMAN'S PATENT DRAWING REVIEW, Form PTO-948, attached to Paper No. 2.

To the extent necessary, Applicant(s) petition for an Extension of Time under 37 C.F.R. 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 08-0870 (118/28508CO) and please credit any excess fees to such deposit account.

Respectfully submitted,

LAW OFFICES OF CHARLES E. WANDS

Charles E. Wands
Reg. No. 25,649

CEW:cn
(407) 725-4760

118/28508CO

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: James D. Beasom

Serial No.: 07/705,~~059~~ 509 Group: 2508

Filed: 05/24/91 Examiner: R. Potter

For: HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

Batch No.: H31

CERTIFICATE OF MAILING

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

March 12, 1993

Sir:

I hereby certify that a LETTER TO DRAFTSMAN, seven (7) sheets of formal drawings, and a 2-month Request for Extension of Time in reply to the Notice of Allowability dated *, to which a reply is currently due on or before March 20, 1993, in connection with the above-identified application is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Honorable Commissioner of Patents and Trademarks, Washington, D.C. 20231 on March 12, 1993.

Charles E. Wands
Reg. No. 25,649

5264719

705509

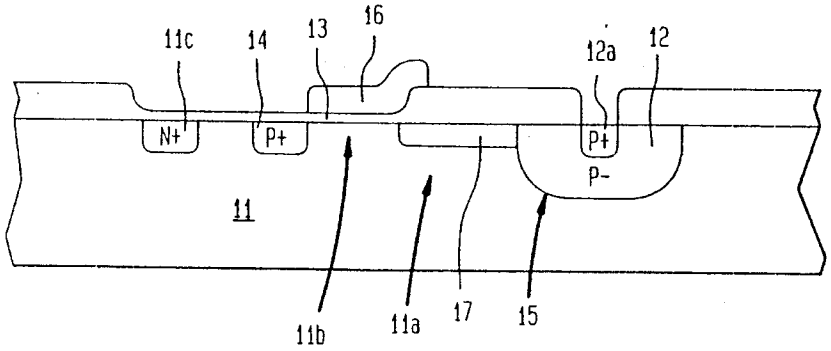


FIG. 1

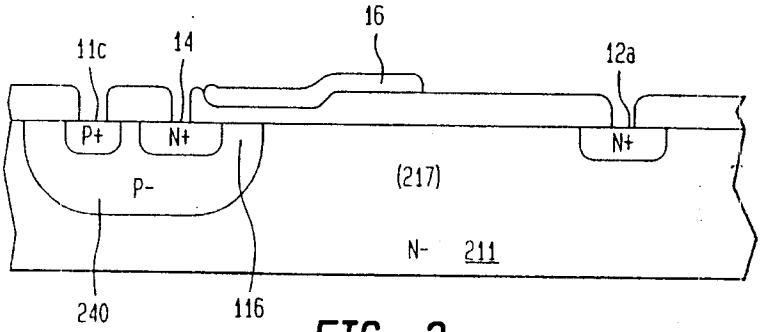


FIG. 2
(PRIOR ART)

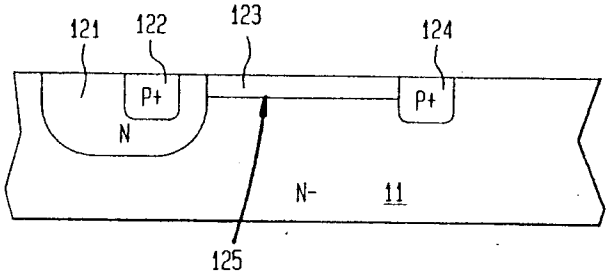


FIG. 3

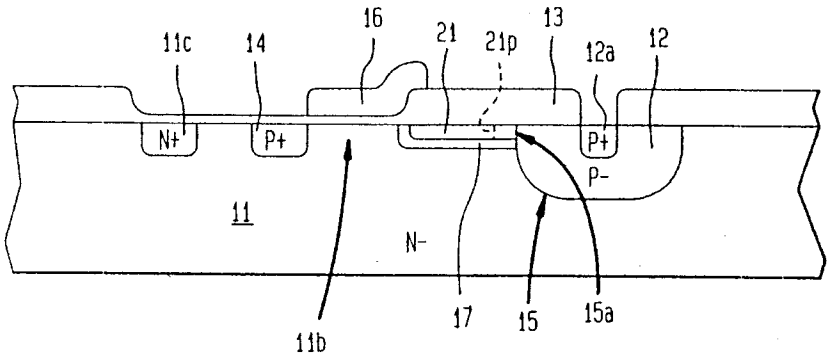
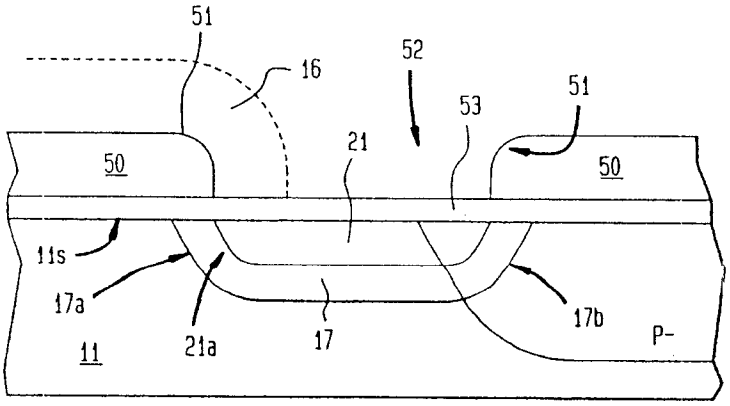

11c
14
16
21
21p
13
12a
12
N+
P+
P+
P-
11
N-
11b
17
15
15a

FIG. 4


51
16
52
53
51
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50
50
11s
17a
17b
P-
11
21a
17

FIG. 5

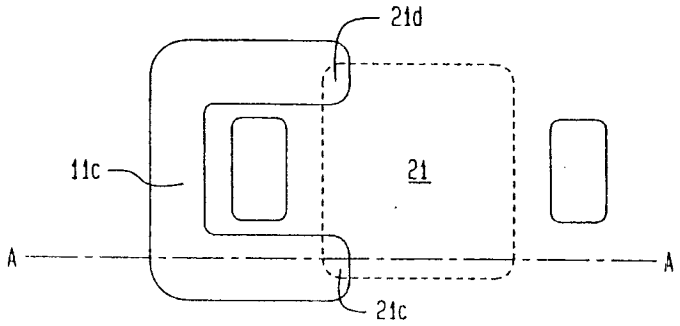


FIG. 6a

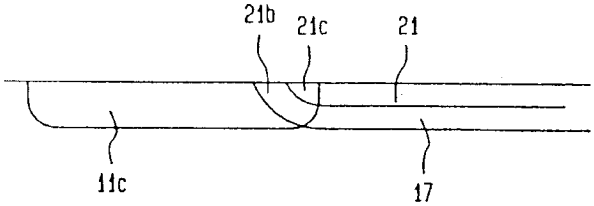


FIG. 6b

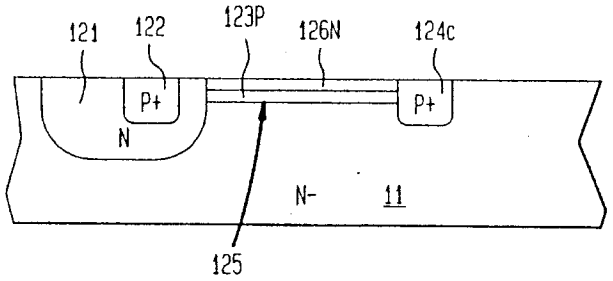

121
122
123P
126N
124c
P+
P+
N
N-
11
125

FIG. 7

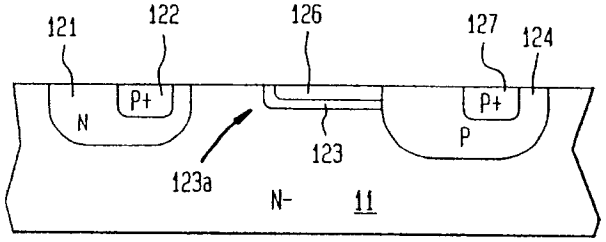

121
122
126
127
124
P+
P+
N
P
123
123a
N-
11

FIG. 8

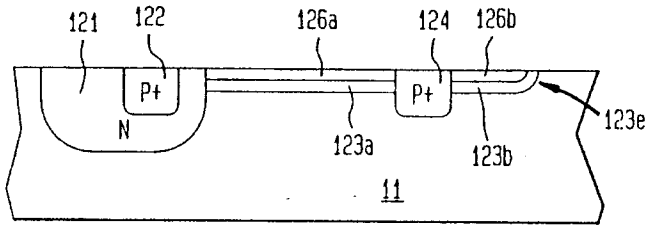
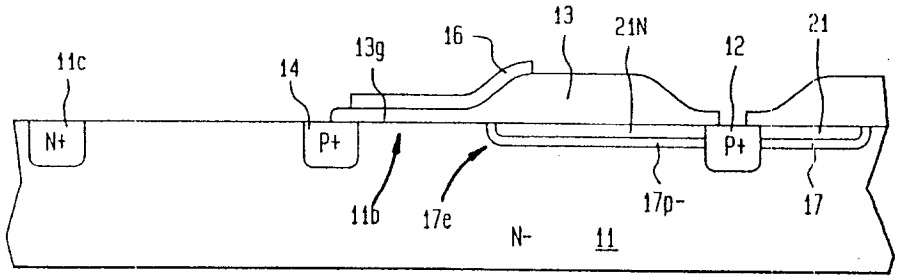

121
122
126a
124
126b
P+
P+
N
123a
123b
123e
11

FIG. 9


11c
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13g
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21N
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N+
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11b
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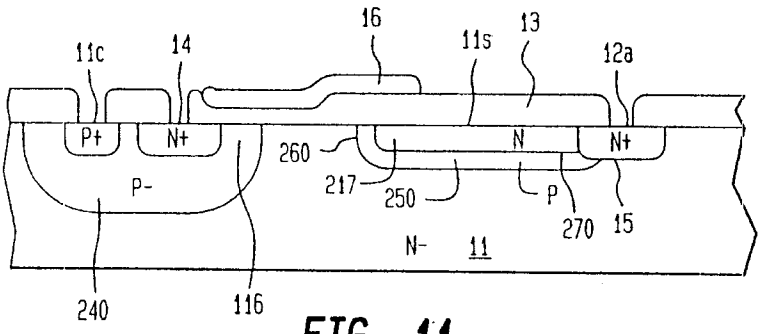
17p-
17
N-
11

FIG. 10


16
11c
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11s
13
12a
P+
N+
260
N
N+
P-
217
250
P
270
15
N- 11
240
116

FIG. 11

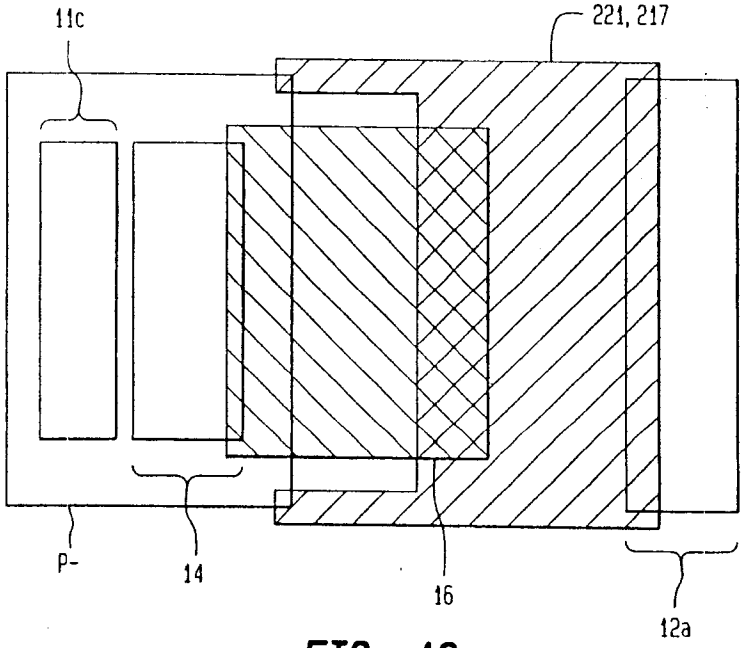

11c
221, 217
P-
14
16
12a

FIG. 12

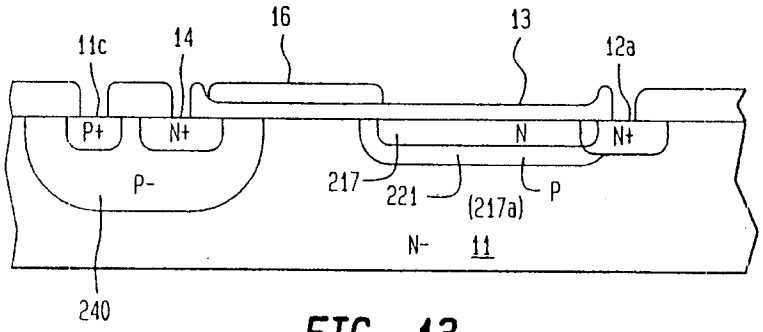
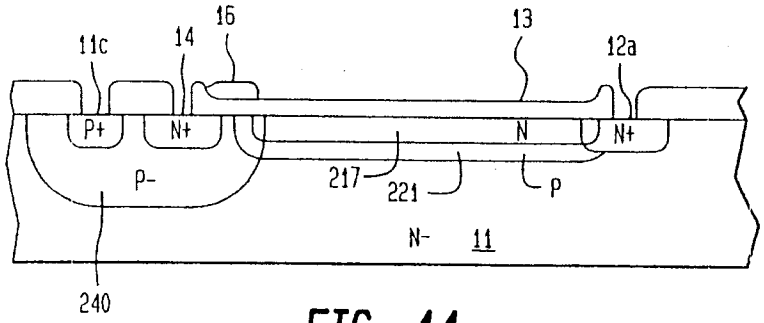

16
13
11c
14
12a
P+
N+
N
N+
P-
217
221
(217a)
P
N- 11
240

FIG. 13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13
11c
14
12a
P+
N+
N
N+
P-
217
221
P
N- 11
240

FIG. 14

118/28508CO

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: James D. Beasom

Serial No.: 07/705,~~039~~ 509 Group: 2508

Filed: 05/24/91 Examiner: R. Potter

For: HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

Batch No.: H31

PETITION FOR EXTENSION OF TIME

Honorable Commissioner of
Patents and Trademarks

March 12, 1993

Sir:

Pursuant to the revised procedures and fee schedules initiated October 1, 1982, Applicant hereby petitions for an Extension of Time for two (2) months until March 20, 1993 for filing formal drawings in reply to the Notice of Allowance dated October 20, 1992, in connection with the above-identified application.

Please charge extension of time fees, and any other fees due in connection with matter to Deposit Account No. 08-0870 (118/28508CO) and please credit any excess to such deposit account.

Respectfully submitted,

LAW OFFICES OF CHARLES E. WANDS

Charles E. Wands
Reg. No. 25,649

To the Comm. of Pats. & Tmks.
Washington, D.C. 20231

Date 3/12/93
Docket No. 28508CO
Serial No. 705,059
Applicant: Beasom

Please confirm receipt of the document(s) checked below by applying your date stamp (and Serial No.):

_____ **PATENT** Appln: spec. _____; claims _____; abstract _____
_____ Infl. Dwgs. _____ Sheets
_____ Power of Atty/Declaration
_____ Response to Office Action , dated _____
_____ Notice of Appeal
_____ Submission of Documents
_____ PTOL Form 85B (issue fee)
_____ Maint. Fee Trans. _____ yr.
_____ Stm. of Use
X_____ Other (describe):
Letter to Draftsman

_____ Verified Stmt.
_____ Filing Fee $ _____
_____ Assign. & Fee
_____ Cert. of Express Mail
X_____ Req. Ext. of Time 2 months
_____ Brief
X_____ Formal Dwgs. 7 shts.
_____ Fee of $ _____ for _____
_____ Trademark Application
_____ Specimens
_____ PCT

PTO UTILITY GRANT
Paper Number 10

The United States of America

The Commissioner of Patents and Trademarks

Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.

Therefore, this

United States Patent

Grants to the person or persons having title to this patent the right to exclude others from making, using or selling the invention throughout the United States of America for the term of seventeen years from the date of this patent, subject to the payment of maintenance fees as provided by law.

Bruce Lehman

Commissioner of Patents and Trademarks

Attest

PTO-1584

FCS1689024

FPI-LOM

STAPLE ARE:

U.S. GOVERNMENT PRINTING OFFICE: 1992-327-409

PATENT NUMBER

ORIGINAL CLASSIFICATION

CLASS	SUBCLASS
257	335

APPLICATION SERIAL NUMBER
07/705509

APPLICANT'S NAME (PLEASE PRINT)
Bergsom

IF REISSUE, ORIGINAL PATENT NUMBER

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)			
257	336	339		

INTERNATIONAL CLASSIFICATION

H	01	L		29/81

GROUP ART UNIT: 2508

ASSISTANT EXAMINER (PLEASE STAMP OR PRINT FULL NAME)
Roy Potter

PRIMARY EXAMINER (PLEASE STAMP OR PRINT FULL NAME)
Rolf Hille

PTO 270 (REV. 5-91)

ISSUE CLASSIFICATION SLIP

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

PATENT APPLICATION FEE DETERMINATION RECORD

Application or Docket Number: 70559

CLAIMS AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY FEE
BASIC FEE				$ 315.00	OR		$ 630.00
TOTAL CLAIMS	/ minus 20 =	*	x $10=		OR	x $20 =	
INDEPENDENT CLAIMS	/ minus 3 =	*	x 30 =		OR	x 60 =	
MULTIPLE DEPENDENT CLAIM PRESENT			+ 100 =		OR	+ 200 =	
			TOTAL		OR	TOTAL	630

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
AMENDMENT A	Total	*	Minus	**	=	x $10=		OR	x $20 =	
	Independent	*	Minus	***	=	x 30 =		OR	x 60=	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+ 100 =		OR	+ 200 =	
						TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	
AMENDMENT B	Total	*	Minus	**	=	x $10 =		OR	x $20 =	
	Independent	*	Minus	***	=	x 30 =		OR	x 60 =	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+ 100 =		OR	+ 200 =	
						TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	
AMENDMENT C	Total	*	Minus	**	=	x $10 =		OR	x $20 =	
	Independent	*	Minus	***	=	x 30 =		OR	x 60 =	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+ 100 =		OR	+ 200 =	
						TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875 (Rev. 12-90) For Fees Effective Nov. 5, 1990 Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET
(FOR USE WITH FORM PTO-875)

SERIAL NO. 705509 | FILING DATE 5-24-91
APPLICANT(S)

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
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50						
TOTAL IND.	1					
TOTAL DEP.						
TOTAL CLAIMS	1					

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	IND.	DEP.	IND.	DEP.	IND.	DEP.
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100						
TOTAL IND.						
TOTAL DEP.						
TOTAL CLAIMS						

PTO-1360 (3-78) *MAY BE USED FOR ADDITIONAL CLAIMS OR AMENDMENTS U.S. DEPARTMENT of COMMERCE Patent and Trademark Office

PTO-1130 (REV. 8-87) 07/705509

PALM III APPLICATION FILE DATA CODING SHEET

U.S. DEPARTMENT OF COMMERCE–PATENT & TM OFFICE | PREPARED BY Mason | DATE 6-6-97

FORMAT NO. 2 Serial No.	TYPE APPL	FILING DATE (Month Day Year)	SPECIAL HANDLING	GROUP ART UNIT	CLASS	SHEETS OF DRAWINGS	ASGT?	TOTAL CLAIMS	INDEPENDENT CLAIMS	SMALL ENTITY?	FILING FEE RECEIVED	SECURITY CASE?	FOREIGN LICENSE
07	1	05/24/97	2	253	357	10	N	11	1	0	149.00	N	Y

FORMAT NO. 3 — ATTORNEY DOCKET NUMBER: 118/285.8C0 — Atty's Reg. Nos. ☐ APPL. PAPERS ☐ CODING SHEET

FORMAT NO. 4 Applicant's Name & Address ☐ APPL. PAPERS ☐ CODING SHEET

FORMAT NO. 5 Title of Invention ☐ APPL. PAPERS ☐ CODING SHEET

FORMAT NO. 6&7 Correspondence Address ☐ APPL. PAPERS ☐ CODING SHEET

FORMAT NO. 8

	RECORD		CONTINUITY CODE	PARENT APPLICATION SERIAL NUMBER	PARENT FILING DATE (Month Day Year)	STATUS CODE	PARENT PATENT NUMBER
	RECORD	801	02	07/424,045	09/08/88	2	
	RECORD	802		0			
	RECORD	803		0			
	RECORD	804		0			
	RECORD	805		0			
	RECORD	806		0			
	RECORD	807		0			
	RECORD	808		0			
	RECORD	809		0			
☐ MORE ON SUPPLEMENTAL CODING SHEET	RECORD	810		0			

FORMAT NO. 9

	RECORD		COUNTRY CODE	PCT/FOREIGN APPLICATION SERIAL NUMBER	FILING DATE (Month Day Year)
	RECORD	901			
FOREIGN PRIORITY CLAIMED? ☐ YES ☐ NO	RECORD	902			
	RECORD	903			
	RECORD	904			
	RECORD	905			
	RECORD	906			
☐ APPLICATION PAPERS	RECORD	907			
	RECORD	908			
	RECORD	909			
☐ MORE ON SUPPLEMENTAL CODING SHEET	RECORD	910			

SEARCHED

Class	Sub.	Date	Exmr.
357	38	3/18/92	
357	55	3/18/92	
357	23.8	3/18/92	
357	46	3/24/92	
357	update	10/15/92	
	38	10/15/92	
	55		
	46		
	23.8		

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
357	38	10/16/92	
	46		
	55		
	23.8		

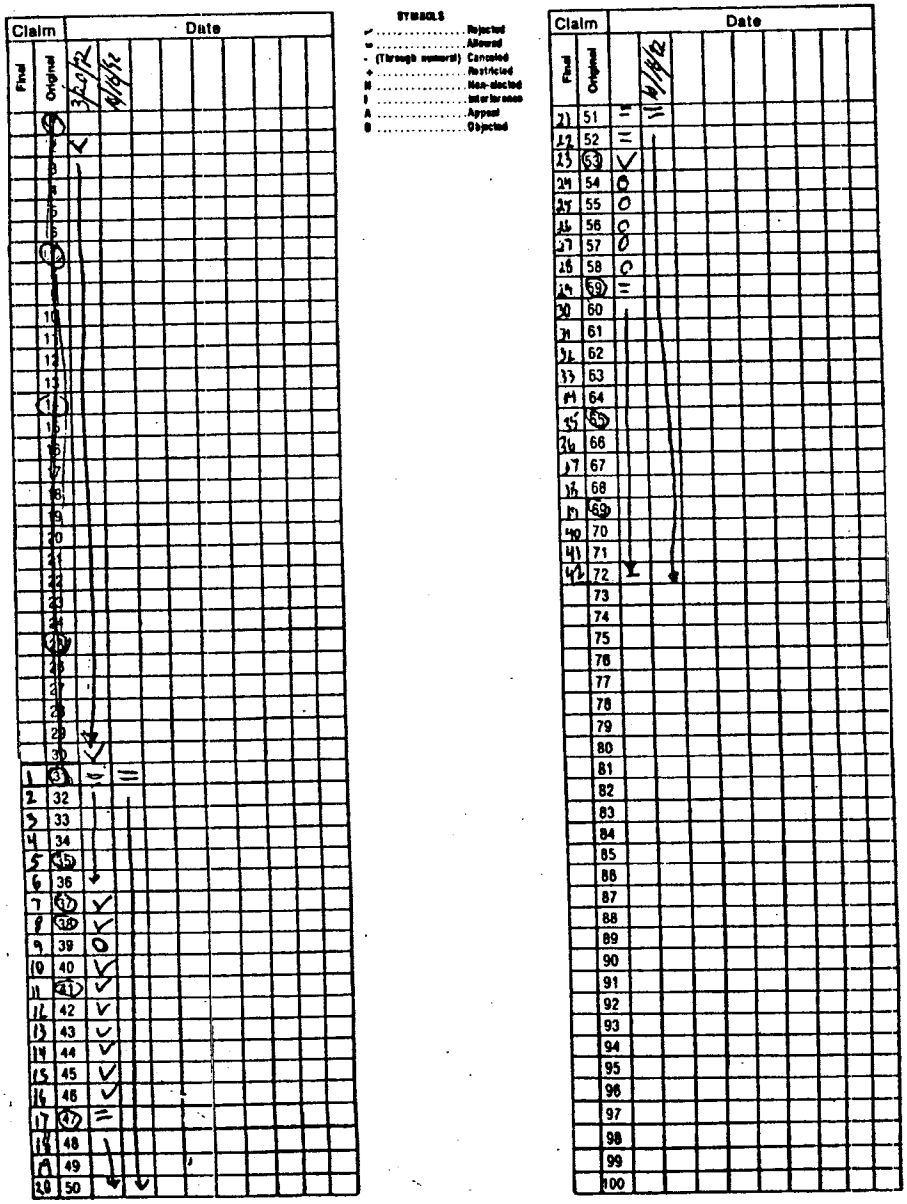
SEARCH NOTES

	Date	Exmr.

Staple Issue Slip Here

POSITION		INIT.	DATE
CLASSIFIER		VE	6/3/91
EXAMINER		24	6-6-91
TYPIST			
VERIFIER			
CORPS CORR.			
SPEC. HAND			
FILE MAINT.			

INDEX OF CLAIMS



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INITIALS

07/705509

Entered or Counted

CONTENTS

Received or Mailed

RECEIVED
JUN 23 1993
GROUP 230

			Received or Mailed
	1.	Application 10 shts papers.	3-24-92
3/20/3	2.	Rec'd Papers	3-24-92
8/13	3.	Addt. Cls	6-29-92
10/19/93	4.	PTOL-37 (Exam	11/27/92
10/5	5.	Change of Firm March 9, 1993	
8/16/93	6.	Issue Fee	Jan 25, 1993
8/11/93	7.	Notice of Abandonment	8/11/93
9/02/93	8.	Notice of Rescinded Abandonment	9/03/93
9/02/93	9.	Re: Abandonment / drawings	Aug 24, 1993
		PTO GRANT NOV 23 1993	
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